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EXAMINER
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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS,
WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 11-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1-9 and 11-29 are pending.

Papers Filed

2:      Examiner acknowledges receipt of amended claims, and amended specification,

all filed 28 March 2006.

Claim Objections

3.   Claims are objected to because of the following informalities:

Claims 11, 13-14 are directed to a processor but depend from a claim

(claim 1) directed toward a method. The claims should be amended to

indicate such in the preamble.

4.   Appropriate correction is required.

New Rejections

Claim Rejections - 35 USC § 112

5.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly
claiming the subject matter which the applicant regards as his invention.

6.   Claims 11 and 13-14 are rejected under 35 U.S.C. 112, second paragraph, as

being indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention.

7.   Claim 11 recites the limitation "the plurality of processing units" in line 2. There is

insufficient antecedent basis for this limitation in the claim. For purposes of

examination, examiner will interpret claim to read "...a plurality of processing units..."

8.   Claim 13 recites the limitations "said plurality of processing units" and "the first

DMA unit" in lines 2-5. There is insufficient antecedent basis for this limitation in the

claim. For purposes of examination, examiner will interpret claim to read "...a plurality of

processing units..." and "...a first DMA controller...".

9.   Claim 14 is rejected on the basis of its dependency to claim 13.

Claim Rejections - 35 USC § 102

10.   The following is a quotation of the appropriate paragraphs of 35

U.S.C. 102 that form the basis for the rejections under this section made in this Office

action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11.   Claims 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Gove.

12.   As per claim 27, Gove discloses a data processor comprising: means for

translating higher level read and write commands into lower level memory access

commands (Fig. 1 transfer processor 11, Col. 58 lines 39-42); a plurality of means for

consuming data (Fig. 1 processors 100-103, transfer processor 11); means for

implementing programmable data paths to supply data to and accept data from any one

of said plurality of data consumption means (*The examiner asserts that in response to instructions, the parallel processors make reads and writes to and from memory to exchange data*); means for receiving instructions, from other than said plurality of data consumption means, to configure the programmable data path implementation means, the plurality of data consumption means, and the higher level read and write translation means (*Master Processor 12 and col. 13 lines 25-35*); and means for implementing a programmable control path through said plurality of data consumption means (Fig. 1 transfer processor 11) to transfer higher level read and write commands from one of said plurality of data consumption means to the higher level read and write translation means. *The examiner asserts that the transfer processor 11 constitutes a data consumption means, as read/write data is consumed as it is translated to interface with external memory. The examiner asserts that packet request signals generated by the processors constitute high-level reads which must be translated to interface with the memory by the transfer processor 11. The similar is true of write commands.*

13.   As per claim 28, Gove discloses the processor of claim 27 further comprising means for ensuring that said lower level memory accesses meet signal level and timing requirements of external memory. *The transfer processor must inherently meet signal and timing requirements of external memory if it is to be successful in carrying out memory transactions. Without successful memory transactions, the invention would be inoperable.*

14.   As per claim 29, Gove discloses the processor of claim 27 further comprising

means for expanding the data processor. (Col. 8 lines 59-61)

Claim Rejections - 35 USC § 103

15.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for

all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

16.   Claims 11, 5-9, 12, and 15-16 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Gove et al. (U.S. Patent No. 5,613,146) hereinafter referred to as

Gove in view of Meeker (U.S. Patent No. 6,073,185).

17.   As per claim 11, Gove discloses the processor of claim 1 but fails to disclose

wherein each of the plurality of processing units has a plurality of control ports on each

side including an input control port and an output control port, and wherein the input

control port of a processing unit is programmable to route incoming command

information to anyone of the output control ports

18.   Meeker discloses wherein each of a plurality of processing units has a plurality of

control ports (Meeker Fig. 3 ports 314-321) on each side including an input control port

(Meeker Fig. 3 ports 314, 316, 318, 320) and an output control port (Meeker Fig. 3 ports

315, 317, 319, 321) (Meeker Col. 7 lines 57-64), and wherein the input control port of a

processing unit is programmable to route incoming command information to anyone of

the output control ports (Meeker Col. 5 lines 57-60) of said processing unit. *The examiner asserts that input data to each processing cell constitutes control data. Input data controls which values are processed by the cell.*

19.   Meeker discloses his invention to "improve computation speed in a SIMD processor" (Col. 2 line 9-10) which is in accordance with a desired outcome of Gove's invention, "faster calculation times" (Col. 1 line 57-58).

20.   It would have been obvious to one of ordinary skill in the art at the time of invention to have included Meeker's processing cell arrangement in Gove's multiprocessor for the benefit of faster calculation times.

21.   As per claim 5, Gove discloses a data processor comprising: a first direct memory access (DMA) unit (Fig. 1 transfer processor 11); and a plurality of processing units (Fig. 1 processors 100-103) each having a plurality of data ports (Fig. 30 ports 3005 and 3006), the data ports being coupled to each other (*The examiner asserts that the ports are connected to each other through the address unit 3001 and data unit 3000)* and programmable to allow data flow from any one of the processing units to another and from any one of the processing units to the DMA unit (Col. 3 line 1-2), wherein one of the processing units has a control port from which it is to send information to the DMA unit about setting up a DMA channel through which one of data to be consumed and result data by one of the processing units is transferred (Col. 37 lines 18-24). *The examiner asserts that data can flow from any processor to any other processor by means of memory.*

22.   Gove fails to disclose each of the plurality of processing units having a plurality of sides, each side having a plurality of unidirectional data ports being an input port and an output port wherein the input port is programmable to route incoming data to any one of the output ports.

23.   Meeker discloses processor cells (Fig. 3 cell 301) having a plurality of sides, each side having a plurality of unidirectional data ports (Fig. 3 ports 314-321) being an input port and an output port. (Col. 7 lines 57-64) wherein the input port is programmable to route incoming data to any one of the output ports. (Meeker Col. 5 lines 57-60)

24.   Meeker discloses his invention to "improve computation speed in a SIMD processor" (Col. 2 line 9-10) which is in accordance with a desired outcome of Gove's invention, "faster calculation times" (Col. 1 line 57-58).

25.   It would have been obvious to one of ordinary skill in the art at the time of invention to have included Meeker's processing cell arrangement in Gove's multiprocessor for the benefit of faster calculation times.

26.   As per claim 6, Gove and Meeker disclose the processor of claim 5 further comprising: memory interface circuitry (Gove Fig. 1 transfer processor 11), wherein the DMA unit is to access external memory via the memory interface circuitry. *The examiner asserts that fig. 1 shows the transfer processor connected to the external memory 15.*

27.   As per claim 7, Gove and Meeker disclose the processor of claim 6 wherein the

memory interface circuitry is on-chip with the DMA unit, the plurality of processing units,

and the host interface. *The examiner asserts that Gove Fig. 1 discloses an on-chip*

region denoted by the hashed line and labeled "ISP Chip Node" which includes the

transfer processor 11, parallel processors 100-103 and host interface 21.

28.   As per claim 8, Gove and Meeker disclose the processor of claim 6 wherein the

memory interface circuitry is designed to interface with external memory. (Gove Fig. 1

and col. 3 line 1-2)

29.   Gove fails to disclose that the external memory is dynamic random access

memory.

30.   Dynamic random access memory (DRAM) is extremely well known to a person of

ordinary skill in the art.

31.   DRAM has the benefits of being cheaper than SRAM and of requiring a smaller

physical space to store an equal amount of data. Cost-minimization is a desired feature

in all processing environments, including that disclosed by Gove.

At the time of invention it would have been obvious to one of ordinary skill in the art to

have included DRAM as external memory 15 in Gove's image processing invention for

the benefit of lower cost.

32.   As per claim 9, Gove and Meeker disclose the processor of claim 5 wherein each

of the processing units has an input programming element (PE) (Gove Fig. 30 data unit

3000) that can read data from any one of its input ports, an output PE (Fig. 30 data unit

3000) that can write result data to any one of its output ports, and a core PE (Fig. 30

data unit 3000) to execute instructions independently of a data path that is operating

through a pair of the input and output ports of that processing unit (Col. 38 lines 26-47)

The examiner asserts that, as pictured in fig. 30, the local and global data ports allow

input and output of the data unit 3000. Further, as specified in line 40, loads, stores and

operations may all be performed in parallel by the data unit 3000.

33.   As per claim 12, Gove and Meeker disclose the processor of claim 9 further

comprising an interface to an external device, and wherein the output ports of one of

said processing units are coupled to the input ports of an adjacent one of said

processing units except that some of the output ports of an outlying one of said

processing units are coupled to the external device interface. (Meeker Col. 4 lines 33-

35)

34.   As per claim 15, Gove and Meeker disclose the processor of claim 5 further

comprising a central processing unit (Gove Fig. 1 master processor 12) to read and

execute instructions that configure the data ports and the DMA unit (Fig. 1 transfer

processor 11) to create a data channel from one of the processing units to external

memory. (Col. 34 line 60 – col. 35 line 6)

35.   As per claim 16, Gove and Meeker disclose the processor of claim 5 further

comprising a host interface unit (Gove Fig. 1 transfer processor 11) to receive

instructions, from an external host controller (Fig. 3 host 33), that configure the data

ports and the DMA unit to create a data path from one of the processing units to

external memory. (Col. 8 line 67 – Col. 9 line 3)

36.   Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gove.

37.   As per claim 24, Gove discloses the system of claim 23 wherein each of the

processing units has a plurality of control ports that are connected to each other in a

mesh arrangement so that the data channel information, including one of a read and

write command, address, and memory access unit channel identifier, can originate from

any one of the processing units and be routed to the memory access unit via a logical

control channel programmed in the mesh arrangement. *The examiner asserts that the*

packet request signal 3012 (Fig. 30) can originate from any parallel processor in MIMD

mode. Col. 37 lines 17-20 disclose that these signals propagate to the transfer

controller.

38.   Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Gove in view of Taylor et al. (Taylor, D. E., Turner, J. S., Lockwood, J. W. "Dynamic

Hardware Plugins (DPH): Exploiting Reconfigurable Hardware for High-Performance

Programmable Routers", Open Architectures and Network Programming Proceedings,

2001 IEEE 27-28 April 2001, Piscataway, NJ, XP010538879, ISBN: 0-7803-7064-3.

Pages 25-34.) hereinafter referred to as Taylor.

39.   As per claim 13, Gove discloses the [method] of claim 1 but fails to disclose the

processor further comprising: a second DMA unit, wherein there are at least four of a

plurality of processing units, the data ports on a north side of first and second ones of

said four processing units are coupled to a first DMA unit, the data ports on a south side

of third and fourth ones of said four processing units are coupled to the second DMA

unit, and the data ports of a south side of the first and second processing units are

coupled to the data ports of a north side of the third and fourth processing units.

40.   Taylor discloses a multiprocessor comprising: a second DMA unit (Fig. 2 memory

interfaces), wherein there are at least four of a plurality of processing units, the data

ports on a north side of first and second ones of said four processing units are coupled

to a first DMA unit, the data ports on a south side of third and fourth ones of said four

processing units are coupled to the second DMA unit, and the data ports of a south side

of the first and second processing units are coupled to the data ports of a north side of

the third and fourth processing units. *The examiner asserts that two processors are*

shown connected to the first DRAM by means of a memory interface, two others are

connected to a second DRAM. The four processors are interconnected by means of the

application controller.

41.   Taylor discloses his invention to as a "mechanism for implementing hight-performance programmable routers" (Page 1, abstract, line 7-8) and "capable of robust flow-specific processing" (Page 1, introduction, line 4) which are in accordance with Gove's goals of increasing processing and computation speed.

42.   At the time of invention is would have been obvious to one of ordinary skill in the art to have included Taylor's method of including a second memory interface opposite the first in Gove's multiprocessor for the benefit of implementing robust, high-performance processing.

43.   As per claim 14, Gove and Taylor disclose the processor of claim 13 further comprising an interface to an external device, wherein some of the data ports of east and west sides of the processing units are coupled to the external device interface. (Taylor fig. 2)

Maintained Rejections

44.   Applicant has failed to overcome the prior art rejections set forth in the previous Office Action. Consequently, these rejections are respectfully maintained by the examiner and are copied below for applicant's convenience.

Claim Rejections - 35 USC § 102

45.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

46.   Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Gove et

al. (U.S. Patent No. 5,613,146) hereinafter referred to as Gove.

47.   As per claim 1, Gove discloses a data driven processing method, comprising:

        providing a first set of instructions and incoming data to a first processing

unit (Fig. 1 master processor 12), of a data driven processor, to operate upon

said incoming data; *The examiner asserts that Gove's processor is driven by*

instruction data which reads on the term "data driven processor" in its broadest

reasonable definition.

        configuring a data path for transferring data between a second processing

unit (Fig. 1 parallel processor 100) of the data driven processor and external

memory (Fig. 1 memory 15);

        and the first processing unit, in response to recognizing that the first set of

instructions will require one of reading from and writing to external memory,

provides addressing information to a memory access unit of the processor to

enable the transfer of additional data between the external memory and the

second processing unit via said data path. (Col. 34 line 60 – Col. 35 line 6)

48.   As per claim 2, Gove discloses the method of claim 1 wherein the first processing

unit recognizes an image processing motion vector in said first set of instructions, and

said additional data is to be written to the external memory and includes a macro block

generated by the second processing unit based on the motion vector. *The examiner*

asserts that "image processing motion vector" and "macro block" constitute image

processing data. Gove discloses "an image and graphics processor" in his abstract.

49.   As per claim 3, Gove discloses the method of claim 1 wherein the data path is

configured by an external host controller (Fig. 3 host 33 and Col. 8 line 67 – Col. 9 line

3).

50.   As per claim 4, Gove discloses the method of claim 1 further comprising: the first

processing unit providing an indication to the memory access unit of whether the

transfer is one of a read and a write. (Col. 37 lines 18-24) *The examiner asserts that*

telling the transfer processor whether it is to perform a read or write is inherent in

Gove's invention. Without a read/write indication, the processor would not function

correctly.

Claim Rejections - 35 USC § 103

51.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

Claims 17-20, 22-23, 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Gove.

52.   As per claim 17, Gove discloses a system comprising: a host controller (Fig. 3

host 33); external memory (fig. 1 memory 15); a data driven processor having a memory

access unit (fig. 1 transfer processor 11) to interface the external memory, a plurality of

processing units (fig. 1 processors 100-103) each having a plurality of data ports (Fig.

30 ports 3005 and 3006), the data ports being coupled to each other (*The examiner*

asserts that the ports are connected to each other through the address unit 3001 and

data unit 3000) and programmable to allow data flow from any one of the processing

units to another and from any one of the processing units to the memory access unit

(Col. 3 line 1-2), and a host interface unit (Fig. 1 transfer processor 11); to receive

instructions from the external host controller that configure the data ports and the

memory unit to create a data path from one of the processing units through a data

channel to the external memory (Col. 8 line 67 – col. 9 line 3), wherein one of the

processing units has a control port which it uses to write data location information to the

memory access unit (Col. 13 lines 1-7); *The examiner asserts that Gove's processor is*

driven by instruction data which reads on the term "data driven processor" in its

broadest reasonable definition.

53.   Gove fails to expressly disclose one of a rechargeable battery and a fuel cell

coupled to power the external memory, the host controller, and the data driven

processor.

54.   Gove discloses one embodiment of his invention to be a "handheld imaging

personal computer" (Col. 5 line 5-6) Batteries are well known in the field of personal

computers and embedded systems.

55.   Running a device off of a battery allows the device to be used in environments
and situations distant from other power sources. Increased mobility is a beneficial
feature of the invention.

56.   It would have been obvious to one of ordinary skill in the art at the time of
invention to have included batteries for power in the handheld embodiment described by
Gove and depicted in Fig. 51 for the benefit of increased mobility.

57.   As per claim 18, Gove discloses the system of claim 17 wherein the host
controller includes an embedded processor and its associated main memory. *The
examiner asserts that Gove refers to host 33 as a Host Processor (Col. 8 line 67).
Further, a processor inherently has memory associated with it. If it did not, the
processor could not function.*

58.   As per claim 19, Gove discloses the system of claim 17 wherein the coupling of
each pair of data ports from adjacent processing units is a point-to-point connection.
*The examiner asserts that all data ports connect directly with data ports of the memory
10 from figure 1. These connections are made regardless of whether processing units
are adjacent or not.*

59.   Gove fails to teach unidirectional ports on processing units 100-103.

60.   Unidirectional ports are extremely well known in the art and provide the benefit of
allowing simultaneous read/write to a functional unit.

61.   It would have been obvious to one of ordinary skill in the art at the time of

invention to have included unidirectional data ports on parallel processors 100-103 in

place of their bidirectional ports for the benefit of simultaneous read/write.

62.   As per claim 20, Gove discloses the system of claim 19 wherein each of the

processing units has a core programming element (PE) (Fig. 30 data unit 3000) that can

be programmed to execute instructions that operate on incoming data received via an

input data port of that processing unit (Col. 38 lines 26-47), an input PE (Fig. 30 data

unit 3000) that can read data from any one of a plurality of input data ports of that

processing unit, and an output PE (Fig. 30 data unit 3000) that can write data to any

one of a plurality of output data ports of that processing unit. *The examiner asserts that,*

as pictured in fig. 30, the local and global data ports allow input and output of the data

unit 3000.

63.   As per claim 22, Gove discloses the system of claim 17 but fails to disclose that

the data location information that is sent through the control port includes information

about the size and display location of a block of image data.

64.   Image location data and size ensure that the image is properly displayed after

processing is completed.

65.   Including image location and size data would have been obvious to one of

ordinary skill in the art at the time of invention for the benefit of ensuring the image

appears in the proper location on the display.

66.   As per claim 23, Gove discloses a system comprising: external memory (Fig. 1

memory 15); a data driven processor having a memory access unit (fig. 1 transfer

processor 11) to interface the external memory, a plurality of processing units (fig. 1

processors 100-103) each having a plurality of data ports (Fig. 30 ports 3005 and 3006),

the data ports being coupled to each other (*The examiner asserts that the ports are*

connected to each other through the address unit 3001 and data unit 3000) and

programmable to allow data flow from any one of the processing units to another and

from any one of the processing units to the memory access unit (Col. 3 line 1-2), and a

central processing unit (fig. 1 master processor 12) to receive and execute instructions

that configure the data ports and the memory unit to create a data path from one of the

processing units through a data channel to the external memory (col. 13 lines 25-31),

wherein one of the processing units has a control port which it uses to write data

channel information to the memory access unit (Col. 13 lines 1-7);

67.   Gove fails to disclose one of a rechargeable battery and a fuel cell coupled to

power the external memory and the data driven processor.

68.   It would be obvious to include batteries in the handheld embodiment disclosed by

Gove for the reasons previously discussed in the rejection of claim 17.

69.   As per claim 25, Gove discloses the system of claim 23 wherein the coupling of

each pair of data ports from adjacent processing units is a point-to-point connection.

The examiner asserts that all data ports connect directly with data ports of the memory

10 from figure 1. These connections are made regardless of whether processing units

are adjacent or not.

70.   Gove fails to teach unidirectional ports on processing units 100-103.

71.   Unidirectional ports are extremely well known in the art and provide the benefit of

allowing simultaneous read/write to a functional unit.

72.   It would have been obvious to one of ordinary skill in the art at the time of

invention to have included unidirectional data ports on parallel processors 100-103 in

place of their bidirectional ports for the benefit of simultaneous read/write.

73.   As per claim 26, Gove discloses the system of claim 23 wherein each of the

processing units has a plurality of control ports (Fig. 30 ports 3011-3013) that are

coupled to each other and are programmable to allow data channel information to be

sent from any one of the processing units to the memory access unit. (Col. 3 lines 1-2)

74.   Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gove in

view of Meeker (U.S. Patent No. 6,073,185).

75.   As per claim 21, Gove and Meeker disclose the system of claim 20 wherein the

core PE of each processing unit can execute its instructions independently of a data

path that is operating through a pair of said input and output data ports of that

processing unit. (Meeker col. 6 lines 1-7)

76.   Meeker discloses his invention to "improve computation speed in a SIMD processor" (Col. 2 line 9-10) which is in accordance with a desired outcome of Gove's invention, "faster calculation times" (Col. 1 line 57-58).

77.   It would have been obvious to one of ordinary skill in the art at the time of invention to have included Meeker's processing cell arrangement in Gove's multiprocessor for the benefit of faster calculation times.

Response to Arguments

78.   Applicant's amendment to the specification filed 28 March 2006 has been entered.

79.   Applicant's arguments filed on 28 March 2006 have been fully considered but they are not persuasive.

80.   Applicant argues the novelty/rejection of claims 1, 5, 17 and 27 on pages 10-12 of the remarks, in substance that:

"the multiprocessor system described in Gove is not a data driven processor."

"According to the Office Action at page 15, it would have been obvious to have included Meeker's processing cell arrangement in Gove's multiprocessor, for the benefit of faster calculation time. However, this is not likely."

"claim 27 has been amended ... to refer to the programmable control path as being through the plurality of data consumption means. Gove does not teach or suggest such a programmable control path."

81.   These arguments are not found persuasive for the following reasons:

a.   The examiner agrees that Gove is of typical von Neuman-type processor.

However, the claimed invention does not discern between a data-driven and von

Neuman processor. Specifically, the applicant does not claim a processor with

"clockless" architecture or without a program counter. The term "data driven

processor" has been interpreted to its broadest reasonable definition: a

processor which is driven by data. While instructions constitute data, Gove reads

on the claim in its current state.

b.   Applicant discusses replacing the crossbar switch in Gove's processor

with the cell array disclosed in Meeker. Examiner points out that for complex

operations involving multiple steps, it would be beneficial to pass data from a first

processing element to a second processing element without passing the data to

a memory device as a temporary holder. The combination of Meeker and Gove

would provide this benefit by allowing data to move from Gove's memory storage

devices (10) to the processing array, arranged as in Fig. 1 of Meeker, flowing

through components until reaching the output buffer. As to the applicant's

argument that "the cross-bar switch would clearly be a faster transport between

parallel processors" the examiner must respectfully disagree. Hooking two

processing elements directly together, as disclosed in Meeker, would be faster

than passing from the first processor to the crossbar to the second processor.

c.   The examiner asserts that the transfer processor 11 in Gove's invention

constitutes a "data consumption means" along with the rest of the parallel

processors 100-103. As such, Gove still reads on claim 27.

Conclusion

82.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

83.   The following is text cited from 37 CFR 1.111(c): In amending in reply to a

rejection of claims in an application or patent under reexamination, the applicant or

patent owner must clearly point out the patentable novelty which he or she thinks the

claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments

avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Dillon Cody whose telephone number is 571-272-8401.

The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

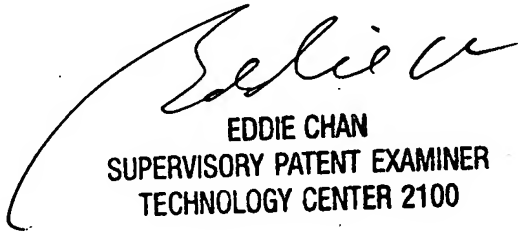Application/Control Number: 10/611,377   Page 24
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

DJC

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